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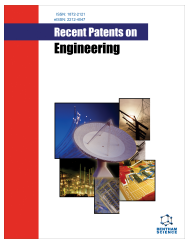
REVIEW ARTICLE

Voltage-Mode First-Order All-Pass Filter With Active Tuning



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Abstract: In this paper, a voltage-mode first-order all-pass filter using three passive components (one capacitor, two resistors) and one active building block (second-generation voltage conveyor) is presented. The proposed design's ideal and non-ideal behaviors are examined to ensure it functions in real-world environments. The effects of variations in capacitance and temperature on the performance of the proposed structure are also analyzed and verified through Monte Carlo simulations. The proposed device gains a patented feature of tunability when NMOS transistors replace two passive resistors with an active equivalent design. Moreover, a second-order all-pass filter is included to test the design's practical viability. The circuit validation is conducted using 0.18 µm CMOS process parameters with a ±0.9 V power supply, using the PSPICE simulation tool, and also validated by experimental setup using IC AD844.

Keywords: All-pass filter, first-order, Monte Carlo simulation, tunability, VCII, voltage-mode.

1. INTRODUCTION

In electronics and communication engineering, a variety of signal-processing applications necessitate different types of frequency-selective circuits. Filters play a crucial role in these applications, including oscillators, communication networks, control systems, video and audio-handling frameworks and biomedical applications. Among various filters, the all-pass filter (APF) is also a fundamental building block for frequency selection. The gain of the APF is unity, meaning it passes all signals without attenuation in magnitude, but the inherent property of the APF is to produce the phase difference between the incoming and outgoing signals. These filters aim to alter the phase response of a signal while minimally impacting its magnitude. Subsequently, literature documents various filters [1-28] capable of passing all signals without attenuation in gain, catering to the diverse needs of analog design engineers. The reported filters are classified into four categories: single input single output [1, 2, 6-28], single input multiple output [3], multiple input single output [4], and multiple input multiple output [5]. Among all these categories, single input single output configurations are particularly popular due to their versatility and simplicity. Achieving optimal performance in APFs, involves considerations such as input impedance, frequency response, and power consumption. Various active building blocks (ABBs) have been explored in APF designs, each offering unique advantages and trade-offs. Common ABBs include current conveyors, operational amplifiers, and transconductance amplifiers, among others. The choice of ABB also significantly influences the performance characteristics of the APF, including bandwidth, linearity, and noise performance. Prior research has investigated different ABB configurations and their impact on APF performance. In [6], an all-pass filter design utilizing a first-generation current conveyor is presented. In [7], a circuit with an inverting second-generation current conveyor features one capacitor and one resistor. In [8], a design using two differential voltage current conveyors is reported, incorporating one capacitor and one resistor. The circuit in [9] includes a modified second-generation current conveyor with two capacitors and one resistor. In [10], a configuration with a universal voltage conveyor consists two capacitors, one resistor, and provides tunability. The design in [11] employs a differential second-generation current conveyor with two capacitors and one resistor. The circuit in [12] uses a differential difference current conveyor, implemented on an advanced technology node with three capacitors and one resistor. In [13], a design with a differential difference dual-X second generation current conveyor is reported, using no capacitors and one resistor. In [14], an extended design with an extra-X second-generation current conveyor is presented, utilizing one capacitor and one resistor. The work in [15] presents a subtractor-based circuit in voltage mode, incorporating one capacitor and one resistor with moderate power consumption. In [16], another design

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with an extra-X second-generation current conveyor is presented, utilizing one capacitor. In [17], a circuit using a voltage differencing current conveyor with two capacitors and one resistor is discussed. The configuration in [18] is based on a current feedback operational amplifier with five or six resistors and one capacitor. In [19], a simple voltage-mode circuit utilizing an operational transconductance amplifier with one capacitor and one resistor is presented. In [20], a dual-X current conveyor differential-input transconductance amplifier is used, with one capacitor and one resistor. The design in [21] employs a current feedback operational amplifier with one capacitor and one resistor. In [22], a voltage differencing differential-input buffered amplifier is utilized. The circuit in [23], utilizing a differential difference dual-X second generation current conveyor, employs a capacitor. In [24], a circuit based on extra-X second generation current conveyor is implemented with additional passive components. The designs in [25] and [26] utilize two active building blocks: a positive differential current conveyor and a differential voltage current conveyor, respectively. The design in [27] uses a simple architecture with a first-generation current conveyor with three resistors and one capacitor. However, despite these advancements, challenges remain in achieving optimal performances in terms of frequency response, power efficiency, and design complexity. Addressing these challenges requires a deeper understanding of the underlying circuit topologies, active building blocks, and optimization techniques. Table **1** shows the detailed comparison between the proposed design and voltage-mode referenced literature.

In this context, this paper aims to contribute to the ongoing research in APF design by proposing a voltage mode first order all-pass filter (VM-FOAPF). The proposed design achieves a compact and efficient circuit implementation by using a single second-generation voltage conveyor (VCII). By minimizing the number of active and passive components, the proposed VM-FOAPF offers improved performance metrics such as reduced power consumption, enhanced frequency response, and greater tunability. The effectiveness of the proposed design is demonstrated through detailed theoretical analysis and simulation studies, highlighting its potential for practical applications in various signal processing systems.

Table 1. Comparison between proposed design and existing literature.

REFERENCE	MODE OF OPERATION	ABB COUNT	ABB TYPE	NO. OF MOS TRANSISTORS	RESISTOR (R)	CAPACITOR (C)	FREQUENCY (Hz)	POWER (W)	SUPPLY (V)	TECHNOLOGY USED (µm)	TUNABILITY	EXPERIMENTAL VALIDATION	MATCHING CONDITION
[6]	VM	--	CCI	--	2	2	--	--	--	--	NO	NO	YES
[7]	VM	1	ICCII	16	1	1	370 k	--	±2.5	0.5	NO	YES	YES
[8]	VM	2	DVCC	36	2	1	1.5 M	--	±2.5	0.5	NO	NO	YES
[9]	VM	1	MCCII-	21	2	1	1 M	--	±2.5	0.35	NO	NO	YES
[10]	VM	1	UVC	40	2	1	0.795 M	5.84 m	±2.5	0.35	YES	YES	YES
[11]	VM	1	DCCII	21	2	1	398 k	14.3 m	±2.5	0.35	NO	YES	YES
[12]	VM	1	DDCC	12	3	1	318.3 k	--	±0.9	0.18	NO	NO	YES
[13]	VM	1	DD-DXCCII	39	0	1	6 M	--	±1.25	0.25	YES	NO	NO
[14]	VM	1	EXCCII	17	1	1	30 M	--	±1.25	0.25	NO	YES	NO
[15]	VM	2	SUBTRACTOR	20	1	1	6.37 M	1.77 m	±0.75	0.13	NO	YES	NO
[16]	VM	1	EXCCII	--	0	1	8.55 M	--	--	0.25	YES	NO	YES
[17]	VM	1	VDCC	16	2	1	1 M	0.492 m	±0.9	0.18	YES	NO	YES
[18]	VM	2	CFOA	--	5	1	79.6 k	0.26 m	±10	--	NO	YES	YES
		3			6	1	79.6 k	0.39 m		--	NO	YES	YES
[19]	VM	2	OTA	16	1	1	8.05 k	0.047 m	±0.4	0.18	YES	YES	YES
[20]	VM	1	DXCCDITA	32	0	1	318 k	--	±1.25	0.35	YES	YES	NO
[21]	VM	2	CFOA	--	3	1	32.15 k	--	±8	--	YES	YES	YES
				--	4	1	31.45 k	--		--	YES	YES	YES
[22]	VM	1	VD-DIBA	--	2	1	159.15 k	--	±5	--	YES	YES	YES
[23]	VM	1	DD-DXCCII	31	0	1	76 M	--	±1.25	0.18	YES	NO	NO
[24]	VM	1	EXCCII	23	2	2	3.18 M	0.7 m	±1.2	0.25	NO	NO	YES
[25]	VM	2	DDCC+	76	1	1	531.2 k/536.1 k	1.8 m	±0.9	0.18	NO	YES	NO
[26]	VM	2	DVCC	24	2	1	1.59 M	--	±2.3	0.5	NO	NO	YES
[27]	VM	1	CCII	5	3	1	4.54 M	0.83 m	±0.75	0.13	NO	YES	NO
PROPOSED (Fig. **3**)	VM	1	VCII	18	2	1	1.59 M	0.69 m	±0.9	0.18	NO	YES	YES
PROPOSED (Fig. **8**)	VM	1	VCII	20	0	1	2.36 M	0.66 m	±0.9	0.18	YES	NO	YES

2. OVERVIEW OF SECOND-GENERATION VOLTAGE CONVEYOR

Second-generation voltage conveyor represents a significant advancement in analog circuit design, offering enhanced functionality over their predecessors, first-generation voltage conveyor (VCI). With additional features, such as working capabilities at higher frequencies and exceptional performance characterized by low distortion, high slew rate, and wide bandwidth, meeting the demands of modern signal processing requirements makes VCII highly versatile and can be extensively used in a wide range of electronic systems [28-36]. VCII's ability to function in both voltage-mode and current-mode configurations further expands its utility, enabling designers to adapt it to diverse applications in active filters, oscillators, instrumentation amplifiers, and voltage-controlled oscillators. VCII is basically a dual current conveyor; on the input side, it acts as a current buffer, while on the output side, it behaves as a voltage buffer with unity gain when the ideal condition is considered [28]. Owing to its inherent features, VCII has been employed in the proposed design as a basic building block. However, it is to be noted that the VCII employed in the proposed VM-FOAPF only requires one X terminal in comparison to the VCII reported in [28] in which two X terminals are used. Fig. (**1**) shows a schematic representation of the three-terminal VCII. Fig. (**2**) shows the internal structure of VCII, which is implemented using complementary metal oxide semiconductor (CMOS) technology.

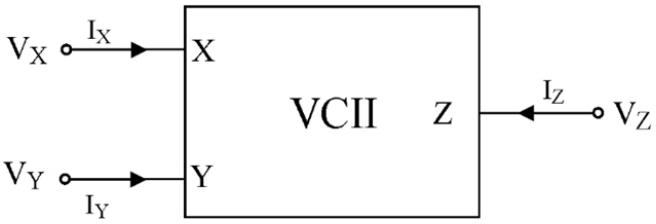

Fig. (1). Schematic representation of VCII [28].

The ideal terminal characteristics *i.e.,* current-voltage relationship between input and output terminals represented by a matrix are described in Eq. (1).

$$\begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} \quad \textbf{(1)}$$

Where, V_X, V_Y, and V_Z are the terminal voltages, and I_X, I_Y, and I_Z are the corresponding terminal currents at nodes X, Y, and Z, respectively.

The aspect ratio of each transistor is listed in Table **2**.

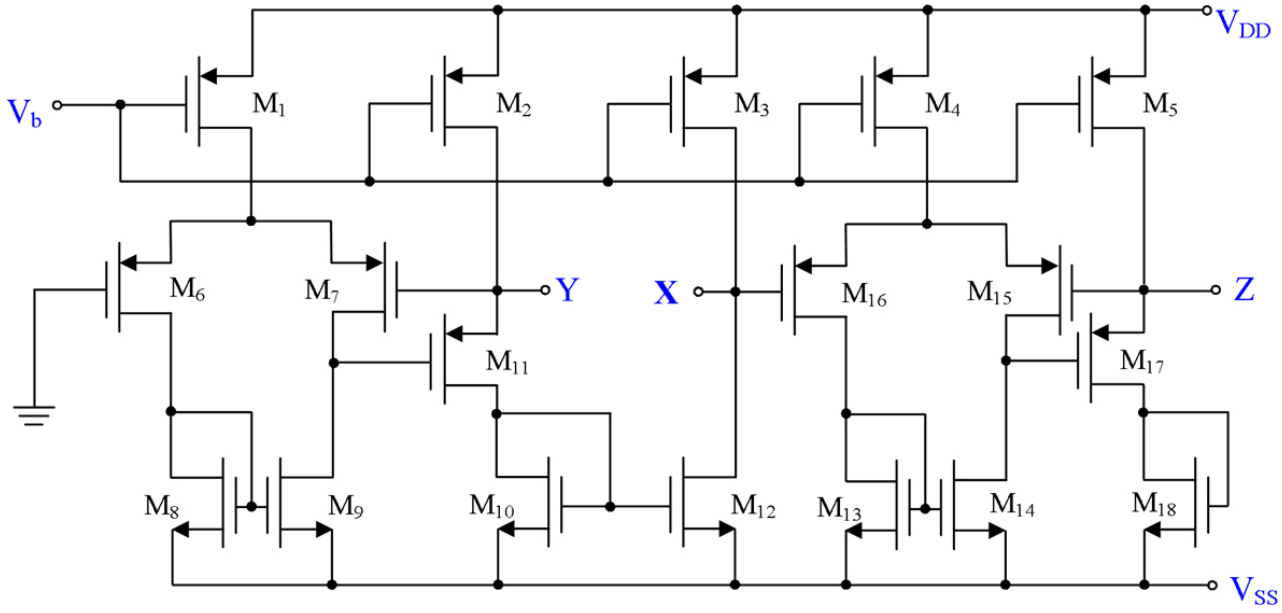

Fig. (2). CMOS Implementation of VCII. *(A higher resolution / colour version of this figure is available in the electronic copy of the article).*

Table 2. Aspect ratios of CMOS transistors.

Transistors	M_1- M_7	M_8 - M_{10}	M_{11} & M_{17}	M_{12} - M_{14}	M_{15} - M_{16}	M_{18}
W(μm)/L(μm)	40.5/0.54	13.5/0.54	81/0.54	13.5/0.54	40.5/0.54	13.5/0.54

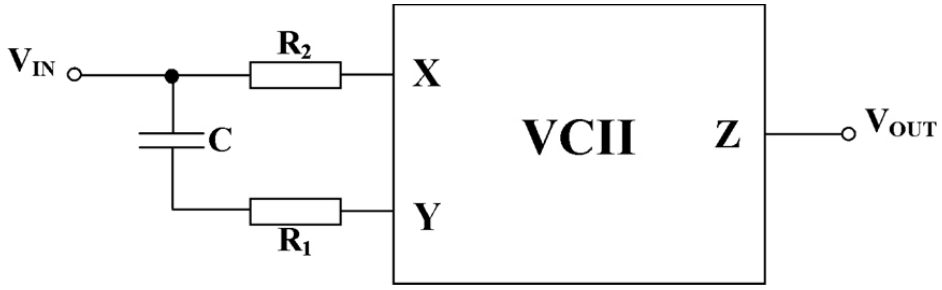

Fig. (3). Proposed VM-FOAPF.

3. PROPOSED ALL-PASS FILTER USING VCII

The proposed design of the VM-FOAPF utilizes a single VCII, a single capacitor (C) and two resistors (R_1 and R_2), as shown in Fig. (**3**).

By analyzing the proposed circuit of VM-FOAPF with the interrelation matrix shown in Eq. (1), the expression for the transfer function is derived and given below as:

$$T_{APF}(s)=\frac{V_{OUT}(s)}{V_{IN}(s)}=\left(\frac{sR_1C-sR_2C+1}{sR_1C+1}\right) \quad \textbf{(2)}$$

The transfer function is modified when $R_2 = 2R_1$, is chosen in the above equation. The modified transfer function of the all-pass filter, which has a gain of unity, pole frequency, and phase difference between the input and output signals, are given by Eqs. (3-5), respectively.

$$T_{APF}(s)=\frac{V_{OUT}(s)}{V_{IN}(s)}=-\left(\frac{sR_1C-1}{sR_1C+1}\right) \quad \textbf{(3)}$$

$$\omega=\frac{1}{R_1C} \quad \textbf{(4)}$$

$$\phi(\omega)=-2\tan^{-1}(\omega R_1C) \quad \textbf{(5)}$$

Eq. (6) provides an indication of the circuit's sensitivity to the resistor and capacitor, which is unity in magnitude. This indicates that the variation in the properties of the passive components has a minimal impact on the extent to which the circuit operates.

$$S_{R_1,C}^{\omega}=-1 \quad \textbf{(6)}$$

4. NON-IDEAL BEHAVIOUR

In the previous section, the ideal behavior model of the VCII is considered, scrutinizing its suitability for analyzing the proposed VM-FOAPF circuit. However, it is imperative to acknowledge the presence of non-ideal characteristics within the VCII, as they can significantly affect circuit performance. Hence, this section focuses on exploring the implications of the non-ideal effects that restrict the voltage transfer gain (β) and current transfer gain (α). The non-ideal nature of both the current transfer gain and voltage transfer gain causes changes in the port relationship, necessitating representation within a matrix form as follows:

$$\begin{bmatrix}I_X\\V_Y\\V_Z\end{bmatrix}=\begin{bmatrix}0&\alpha&0\\0&0&0\\\beta&0&0\end{bmatrix}\begin{bmatrix}V_X\\I_Y\\I_Z\end{bmatrix} \quad \textbf{(7)}$$

Considering the non-idealities in the voltage and current transfer gains as described in Eq. (7), the transfer function can be formulated as given below.

$$T_{APF}(s)_{non-ideal}=\frac{V_{OUT}(s)}{V_{IN}(s)}=\beta\left(\frac{1+sR_1C-s\alpha R_2C}{sR_1C+1}\right) \quad \textbf{(8)}$$

Under non-ideal situation and with $R_2 = 2R_1$, modified transfer function, pole frequency, phase difference introduced by presented filter and its sensitivity with respect to passive components and non-ideal parameters are given in Eqs. (9-12), respectively.

$$T_{APF}(s)_{non-ideal}=\frac{V_{OUT}(s)}{V_{IN}(s)}=\beta\left(\frac{1+sR_1C(1-2\alpha)}{sR_1C+1}\right) \quad \textbf{(9)}$$

$$\omega_{non-ideal}=\frac{1}{R_1C} \quad \textbf{(10)}$$

$$\phi(\omega)_{non-ideal}=\tan^{-1}(\omega R_1C(1-2\alpha))-\tan^{-1}(\omega R_1C) \quad \textbf{(11)}$$

$$S_{R_1,C}^{\omega}=-1,\ \ S_{\alpha,\beta}^{\omega}=0 \quad \textbf{(12)}$$

5. SIMULATION RESULTS

The functionality of the proposed VM-FOAPF shown in Fig. (**3**) has been validated using Cadence PSPICE simulations. TSMC's 0.18 µm CMOS parameters are employed,

with power supplies of ±0.9 V DC. With a bias voltage of 0.3 V DC, resistances, R_1 equals to 1 kΩ, R_2 equals to 2 kΩ, and the capacitor, C equals to 0.1 nF, the theoretically calculated pole frequency is 1.59 MHz. According to Fig. (**4**), the simulated pole frequency is 1.57 MHz, showing a deviation of 1.25% from the expected value. The theoretical and simulated pole frequencies exhibit a negligible difference within acceptable limits. The proposed filter has a low power consumption of 0.69 mW only. Furthermore, Fig. (**5**) shows the 90° phase shift between the simulated output and the applied input signals. The change in the temperature from 0°C to 100°C, has a minimal effect on the transient and AC responses of the proposed VM-FOAPF. The temperature variations in the transient and frequency responses are illustrated in Figs. (**6**) and (**7**), respectively.

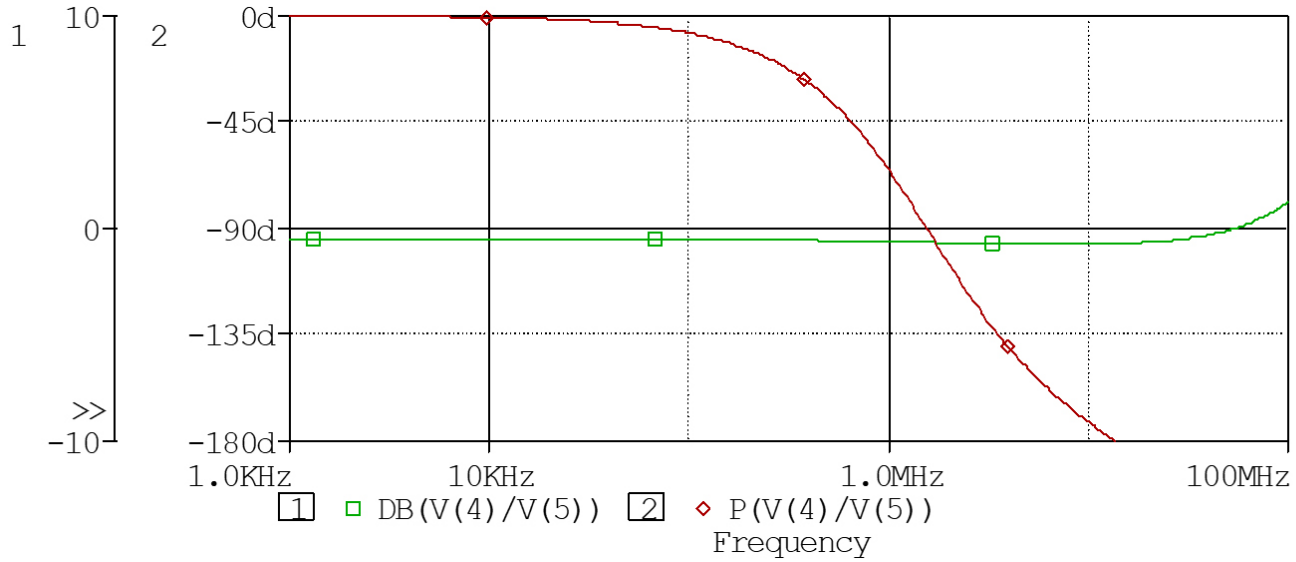

Fig. (4). Frequency responses of the proposed VM-FOAPF. *(A higher resolution / colour version of this figure is available in the electronic copy of the article).*

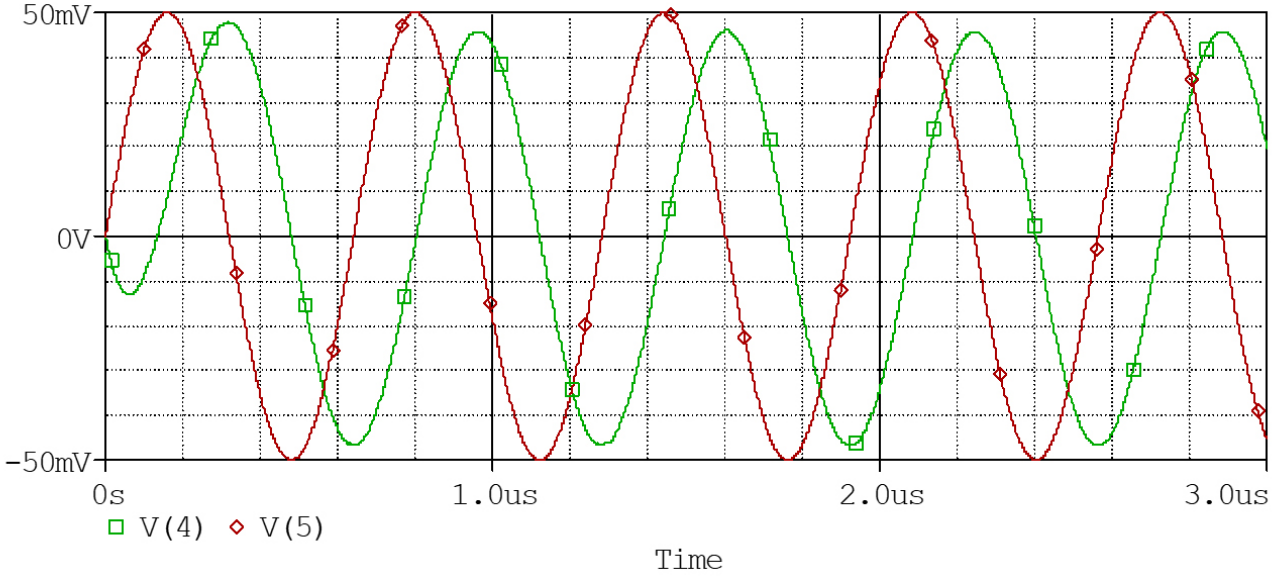

Fig. (5). Transient responses of the proposed VM-FOAPF. *(A higher resolution / colour version of this figure is available in the electronic copy of the article).*

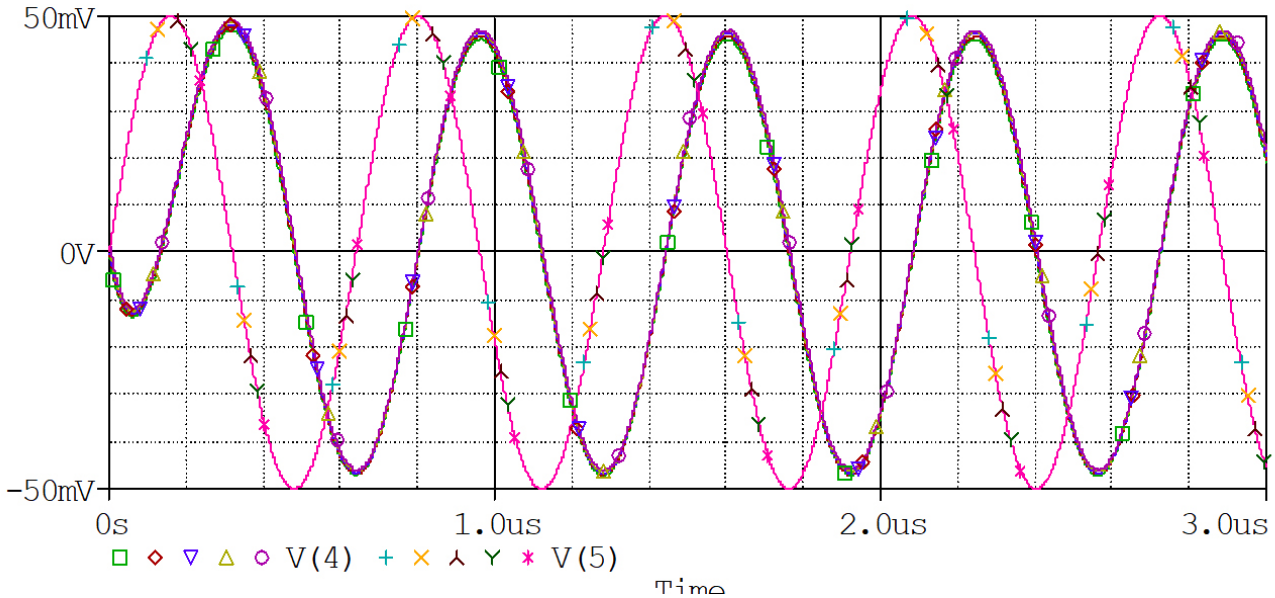

Fig. (6). Impact of temperature on the transient plots of the proposed VM-FOAPF. *(A higher resolution / colour version of this figure is available in the electronic copy of the article).*

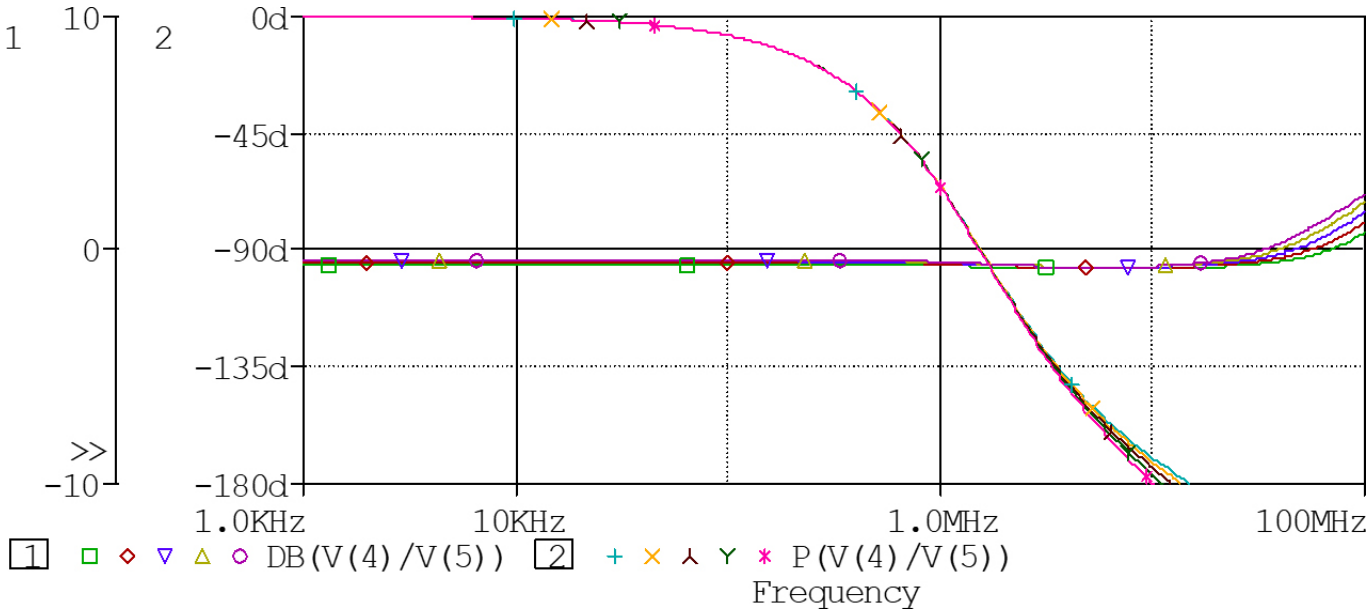

Fig. (7). Impact of temperature on the AC plots of the proposed VM-FOAPF. *(A higher resolution / colour version of this figure is available in the electronic copy of the article).*

6. ACTIVE-C REALIZATION

Filters that do not realize active-C have significant challenges owing to their signal-processing capabilities. For instance, they may exhibit inferior characteristics, including limited roll-off, decreased selectivity, and heightened sensitivity to component tolerances, compared to their active counterparts. A primary concern arises from the inherent limitations of passive components, which offer restricted control over key parameters, such as gain, bandwidth, and Q-factor. This constraint becomes particularly problematic when filters are tailored for applications with specific demands, such as audio processing or communication systems. The absence of precious control over passive components restricts the design from meeting performance criteria, often leading to compromise in other design aspects. Consequent-

ly, achieving the desired results becomes challenging, potentially resulting in suboptimal solutions, and necessitating extensive trial-and-error iterations during the design phase. To solve this problem in the presented design, passive resistors R_1 and R_2 are replaced with NMOS-based active resistors that operate in the triode region, as shown in Fig. (**8**). This can help overcome some of the problems associated with making signal-processing devices without active-C realization. MOS-based active resistors offer several advantages over traditional passive resistors, including greater controllability [13, 16, 30, 37, 38] lower sensitivity to temperature variation, and reduced susceptibility to electromagnetic interference. Eqs. (13) and (14), respectively, show a mathematical description of the resistance produced using NMOS transistors M_{RA} and M_{RB}.

$$R_{MRA} = \left[\mu_n C_{ox} \left(\frac{W}{L} \right)_{MRA} \left(V_{C1} - V_{Tn} \right) \right]^{-1} \quad \textbf{(13)}$$

$$R_{MRB} = \left[\mu_n C_{ox} \left(\frac{W}{L} \right)_{MRB} \left(V_{C2} - V_{Tn} \right) \right]^{-1} \quad \textbf{(14)}$$

Where μ_n represents the mobility of the electron charge carrier, V_{C1} and V_{C2} are the control gate voltages, C_{ox} is the gate oxide capacitance per unit area, L denotes the gate channel length, W signifies the gate width, and V_{Tn} refers to the threshold voltages of NMOS transistors M_{RA} and M_{RB}.

The transfer function and phase angle of the active-C variant of the proposed VM-FOAPF are given in Eqs. (15) and (16), respectively.

$$T_{APF}(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} = -\left(\frac{sR_{MRA}C - 1}{sR_{MRA}C + 1} \right) \quad \textbf{(15)}$$

$$\phi(\omega) = -2\tan^{-1}\left(\omega R_{MRA} C\right) \quad \textbf{(16)}$$

The active-C VM-FOAPF shown in Fig. (**8**) is validated using equal combinations of process parameters, aspect ratios, and supply voltages. The NMOS transistors M_{RA} and M_{RB} are configured with W/L = 1.08 µm/0.54 µm. For simulation purposes, a 0.1 nF capacitor is employed. To achieve resistances of R_{MRA} = 1 kΩ and R_{MRB} = 2 kΩ, the gate control voltages V_{C1} and V_{C2} are adjusted to 0.63 V and 0.54 V. Fig. (**9**) shows the simulated phase and gain responses. If the controlling voltages are varied, then the values of R_{MRA} and R_{MRB} change, causing a change in pole frequency thus tunability feature is added to proposed design. Fig. (**10**) shows the tunability aspect of the proposed active-C VM-FOAPF. The effect of temperature variation from 0°C to 100°C on the frequency response plot for the active-C variant of the proposed VM-FOAPF is illustrated in Fig. (**11**), which reveals that the gain and phase responses remained within the acceptable range across different temperature variations.

The designs of anlog-based circuits are still complex for designers, as there are many factors that may affect the performance of analog circuits, one of which is noise, which can be from any reason, that is, internal and external parameters. Without noise measurements, no analog design can be processed for fabrication. The input and output noises for the proposed design are shown in Fig. (**12**). As the frequency changes, it is observed from the graph that the output noise is less than the input noise. The simulated input and output noises are 0.192 nV/√Hz and 0.178 nV/√Hz, respectively, at the pole frequency. Owing to the passive nature of the capacitor, some variations can affect the pole frequency, which is not desirable. The effect of capacitor variation on the pole frequency can be analyzed using Monte Carlo simulations with 100 runs as shown in Fig. (**13**). The design aspects for analog circuits contain many theories for phase difference analysis, one of which is the Bowditch pattern, as shown in Fig. (**14**). The graph shows that the ratio between the output and input signals is 1:1, and the simulated phase difference between them is 90°, which is the foremost requirement for all-pass filters.

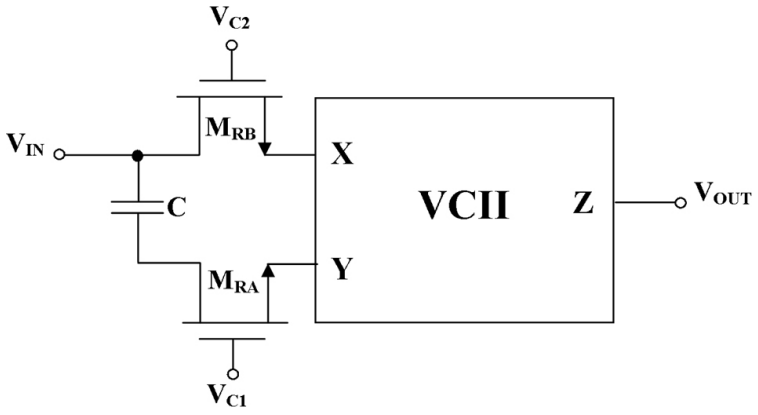

Fig. (8). Proposed active-C VM-FOAPF.

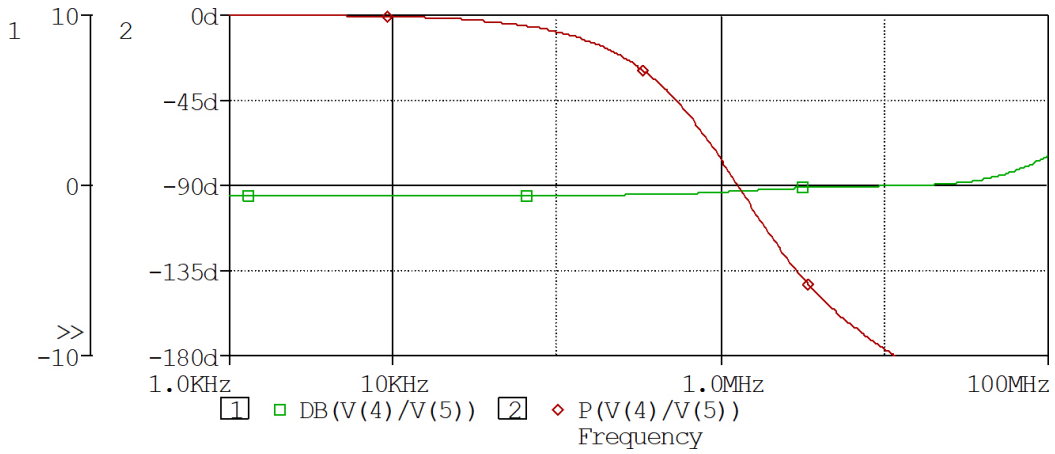

Fig. (9). Proposed active-C VM-FOAPF's simulated phase and gain responses. *(A higher resolution / colour version of this figure is available in the electronic copy of the article).*

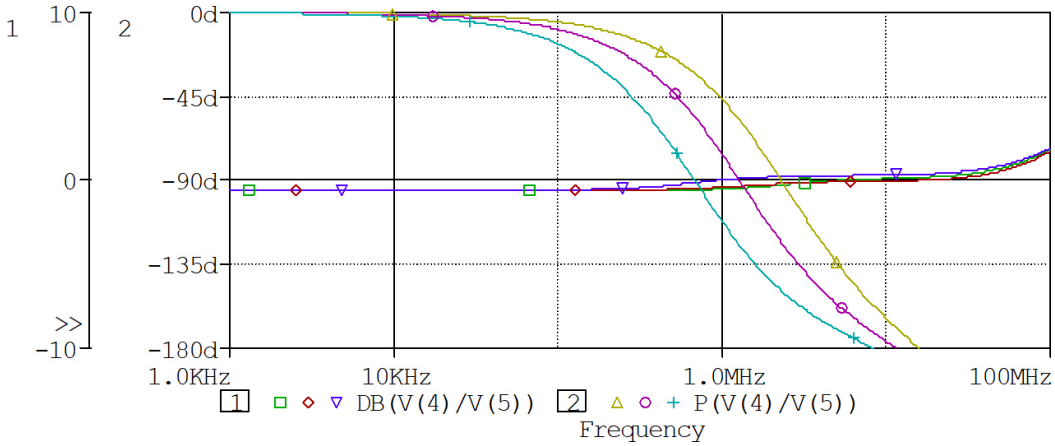

Fig. (10). Tunability feature of the proposed active-C VM-FOAPF. *(A higher resolution / colour version of this figure is available in the electronic copy of the article).*

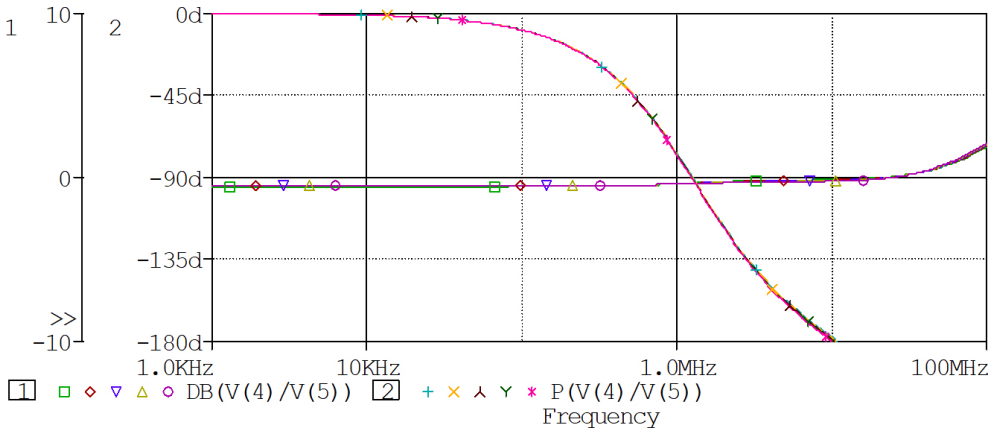

Fig. (11). Temperature effect on proposed active-C VM-FOAPF AC plots. *(A higher resolution / colour version of this figure is available in the electronic copy of the article).*

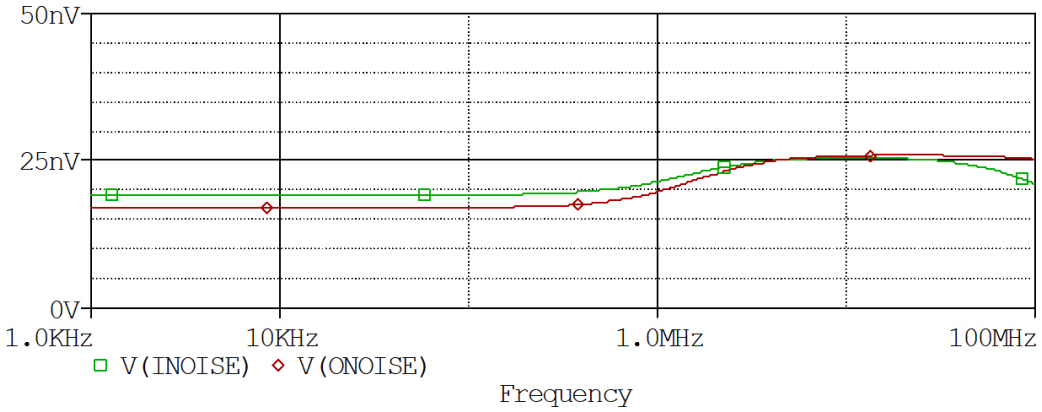

Fig. (12). Noise variation at input and output terminal of proposed active-C VM-FOAPF. *(A higher resolution / colour version of this figure is available in the electronic copy of the article).*

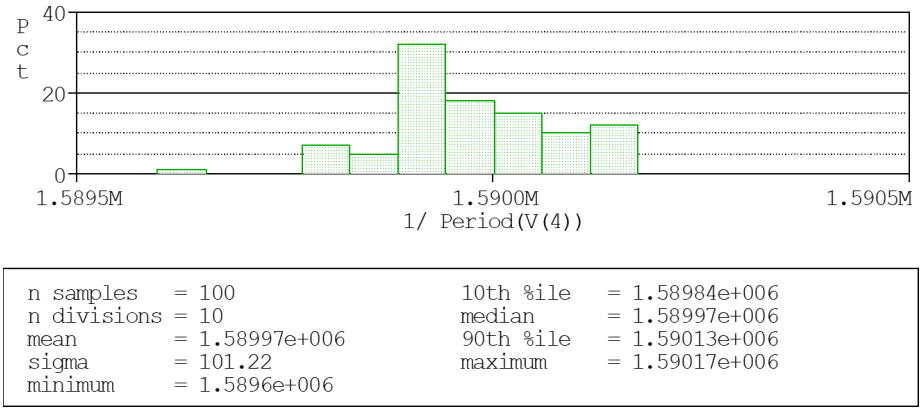

Fig. (13). Monte Carlo plot of the proposed active-C VM-FOAPF. *(A higher resolution / colour version of this figure is available in the electronic copy of the article).*

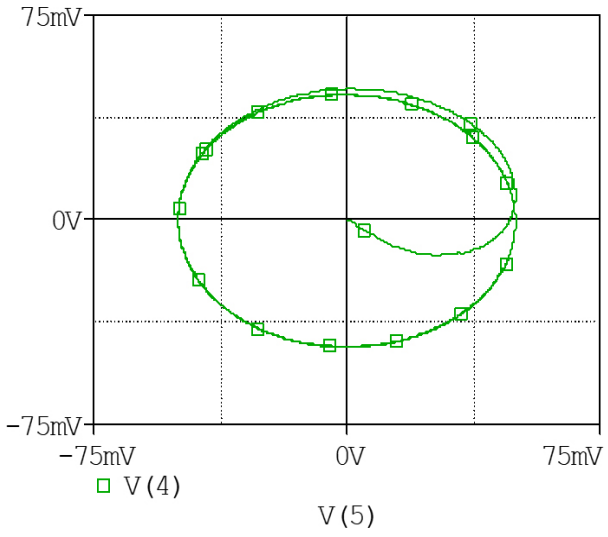

Fig. (14). Bowditch pattern of the proposed active-C VM-FOAPF. *(A higher resolution / colour version of this figure is available in the electronic copy of the article).*

7. APPLICABILITY ASPECTS

According to previous studies, a filter's ability to separate unwanted signals improves in accordance with its complexity. For instance, a second-order filter offers a more refined filtering response compared to a first-order filter, with a stop band slope of -40 dB/decade. Leveraging the cascading property [11, 25, 26, 39] of a first-order all-pass filter allows for the practical and cost-effective construction of a second-order all-pass filter. When designing a higher-order filter using the cascading technique, the impedance level at the input port of the last stage and the impedance level at the output port of the first stage must meet the required impedance-matching conditions. This implies that the impedance characteristics of the first-order filter play an important role in determining the feasibility of a higher-order filter extension. If the first-order filter satisfies these requirements, then only it can be used as a building block for a higher-order filter without the need for additional buffer stages. The voltage mode second order all pass filter (VM-SOAPF) is composed of cascading two VM-FOAPF and is illustrated in Fig. (**15**). In Fig. (**15**), terminal X of VCII has high input

impedance and terminal Z offers low impedance that eliminates the need for extra buffer circuitry. However, the value of R_1 may affect the impedance levels.

Eqs. (17) and (18) represent the transfer function, whereas Eqs. (19) and (20) express the phase angle and pole frequency for VM-SOAPF.

$$T_{APF}(s)=\frac{V_{OUT}(s)}{V_{IN}(s)}=\left(\frac{sR_1C-1}{sR_1C+1}\right)\left(\frac{sR'_1C'-1}{sR'_1C'+1}\right) \quad \textbf{(17)}$$

$$T_{APF}(s)=\frac{V_{OUT}(s)}{V_{IN}(s)}=\left(\frac{s^2R_1R'_1CC'-s\left(R_1C+R'_1C'\right)+1}{s^2R_1R'_1CC'+s\left(R_1C+R'_1C'\right)+1}\right) \quad \textbf{(18)}$$

$$\varphi(\omega)=-2\tan^{-1}(\omega R_1C)-2\tan^{-1}(\omega R'_1C') \quad \textbf{(19)}$$

$$\omega=\left(\frac{1}{R_1C}\times\frac{1}{R'_1C'}\right)^{1/2} \quad \textbf{(20)}$$

According to Eq. (19), a second-order all-pass filter induces a phase shift varying from 0° to -360° across the frequency spectrum. Utilizing identical supply voltages as employed in simulating the first-order APF to validate the proposed second-order APF. Resistors R_1 and R'_1 are set at 1 kΩ, while capacitors C and C' are both configured at 0.1 nF. Fig. (**16**) illustrates the gain and phase responses of the VM-SOAPF. The simulation findings determine the pole frequency as 1.53 MHz. Furthermore, Fig. (**17**) shows the input and output simulated transient responses at the pole frequency.

The phase shift that is provided by each block is added during cascade operation. For instance, the first stage of an all-pass filter introduces a 90° phase shift, and the second stage of a first-order all-pass filter adds another 90°. Consequently, the overall phase difference between the input and output voltage signals of the proposed second-order filter is 180° at its pole frequency.

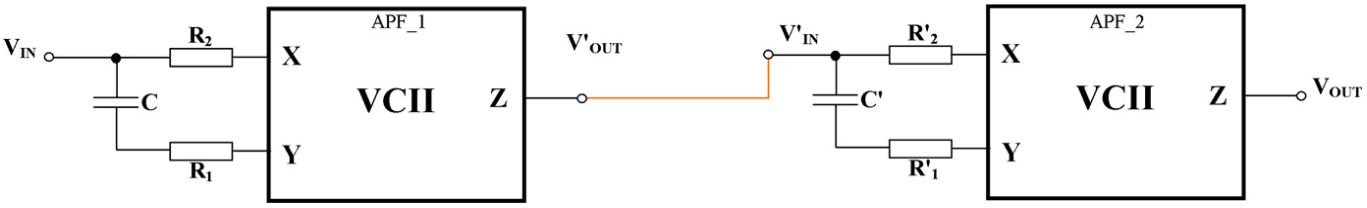

Fig. (15). Implementation of the VM-SOAPF by cascading two VM-FOAPF. *(A higher resolution / colour version of this figure is available in the electronic copy of the article).*

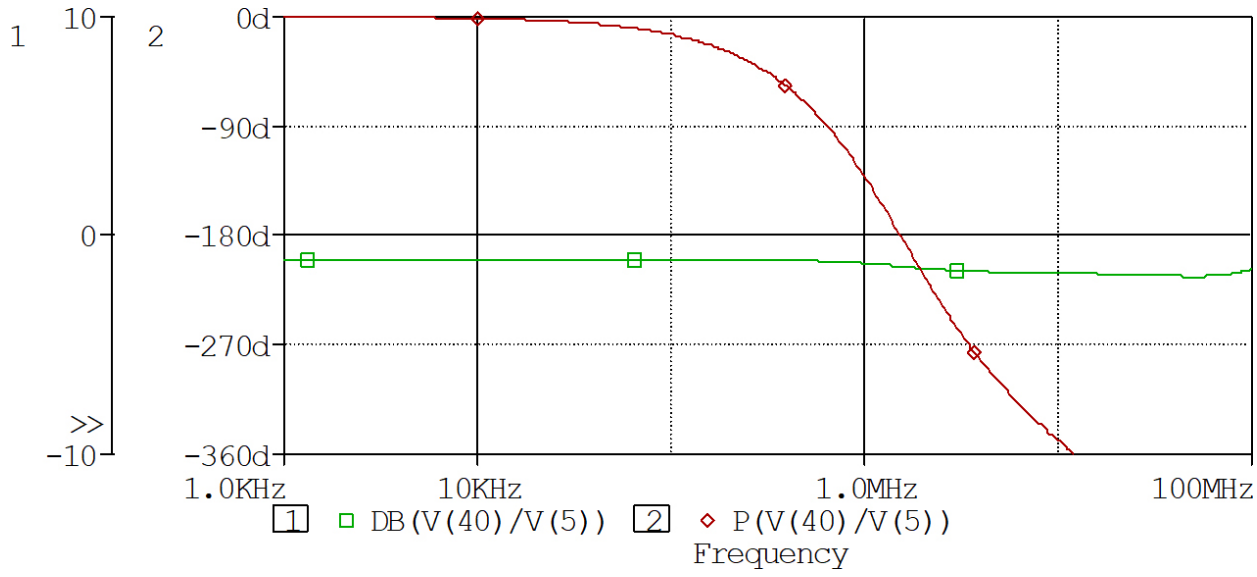

Fig. (16). Frequency responses of proposed VM-SOAPF. *(A higher resolution / colour version of this figure is available in the electronic copy of the article).*

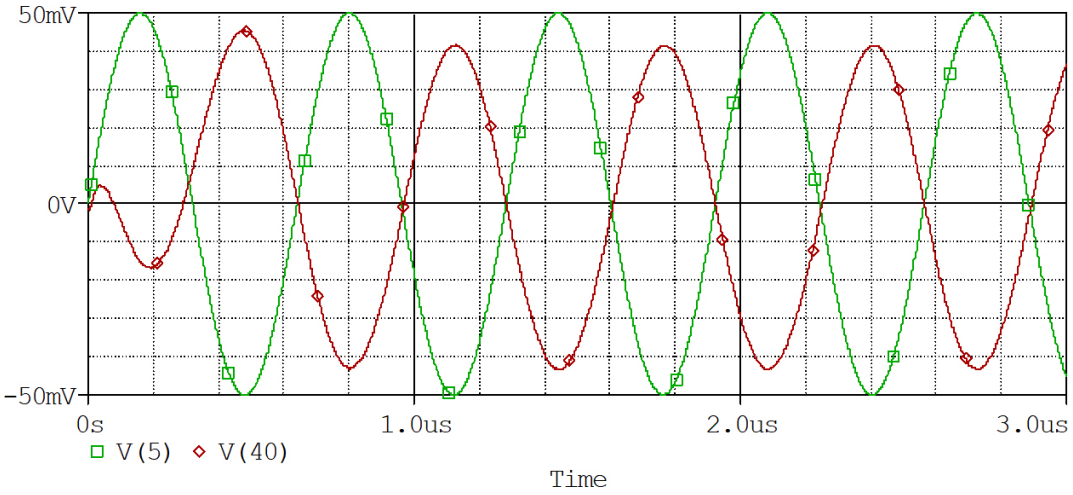

Fig. (17). Transient responses of proposed VM-SOAPF. *(A higher resolution / colour version of this figure is available in the electronic copy of the article).*

8. EXPERIMENTAL VALIDATION

Several integrated circuits are commercially available for designing all-pass filters including, AD830 [40], LT1228 [41], and AD844 [32, 42, 43]. The experimental behavior of the all-pass filter (APF) circuit is examined using the AD844 IC, which is commercially available. The VCII active device can be implemented using the commercially available integrated circuit (IC) AD844, as shown in Fig. (**18**) [32]. The proposed VM-FOAPF is implemented using one AD844 IC, two resistors, and one capacitor, as illustrated in Fig. (**19**). The component values are R_1 = 5 kΩ, R_2 = 10 kΩ, and C = 1 nF. The DC power supply should be within ±10 V.

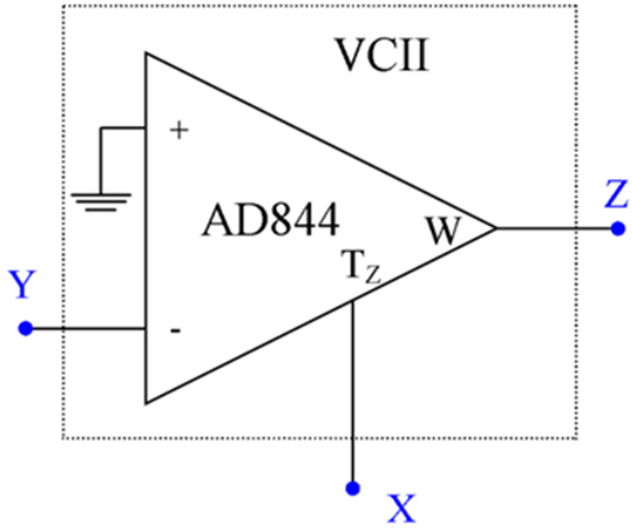

Fig. (18). VCII realization using IC AD844 [32]. *(A higher resolution / colour version of this figure is available in the electronic copy of the article).*

Fig. (**20**) depicts the transient responses of the VM-FOAPF circuit with a 90° phase shift between the output signal waveforms and the applied sinusoidal input. The pole frequency is calculated to be 31.8 kHz. However, variations in the experimental pole frequency may occur due to the parasitic of the IC AD844 and the 5% tolerance of the resistors and capacitors used in the circuit design.

Fig. (**21**) confirms the 90° phase shift between the input and output signals by displaying the phase quadrature relationship in X-Y mode.

CONCLUSION

In this paper, a voltage-mode first-order all-pass filter design using three passive components (two resistors and one capacitor) and an active building block, (VCII) is presented. The design's ideal and non-ideal behaviors are examined to validate its functionality in real-world scenarios. Monte Carlo simulations assess the impact of temperature and capacitance variations on the design's performance. Additionally, an NMOS transistor is integrated to replace a passive resistor, enhancing the design's tunability. The circuit provided is verified using a voltage supply of ± 0.9 V and a 0.18 µm CMOS parameter using the PSPICE tool. Furthermore, an experimental verification is conducted with AD844 ICs to confirm the feasibility of the proposed circuit.

CURRENT AND FUTURE DEVELOPMENTS

The study described in this paper aims to advance the understanding of analog signal processing. As device miniaturization is an essential objective in current electronic devices, several distinct concepts, such as optimized ABB performance and signal processing using oscillators and filters, can be explored further by employing lower technology nodes. Novel ABB can be utilized in the future to develop simple, compact designs that make analog engineering more cost-effective and energy-efficient, in addition to providing cascadable properties and tunability features.

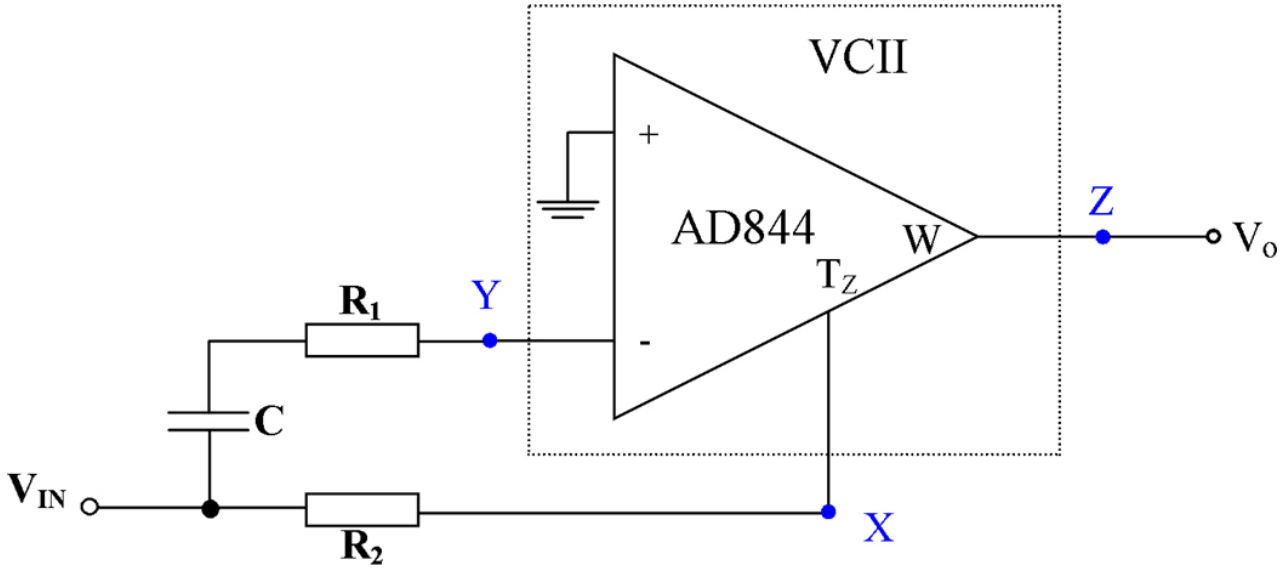

Fig. (19). Experimental implementation of the proposed VM-FOAPF. *(A higher resolution / colour version of this figure is available in the electronic copy of the article)*.

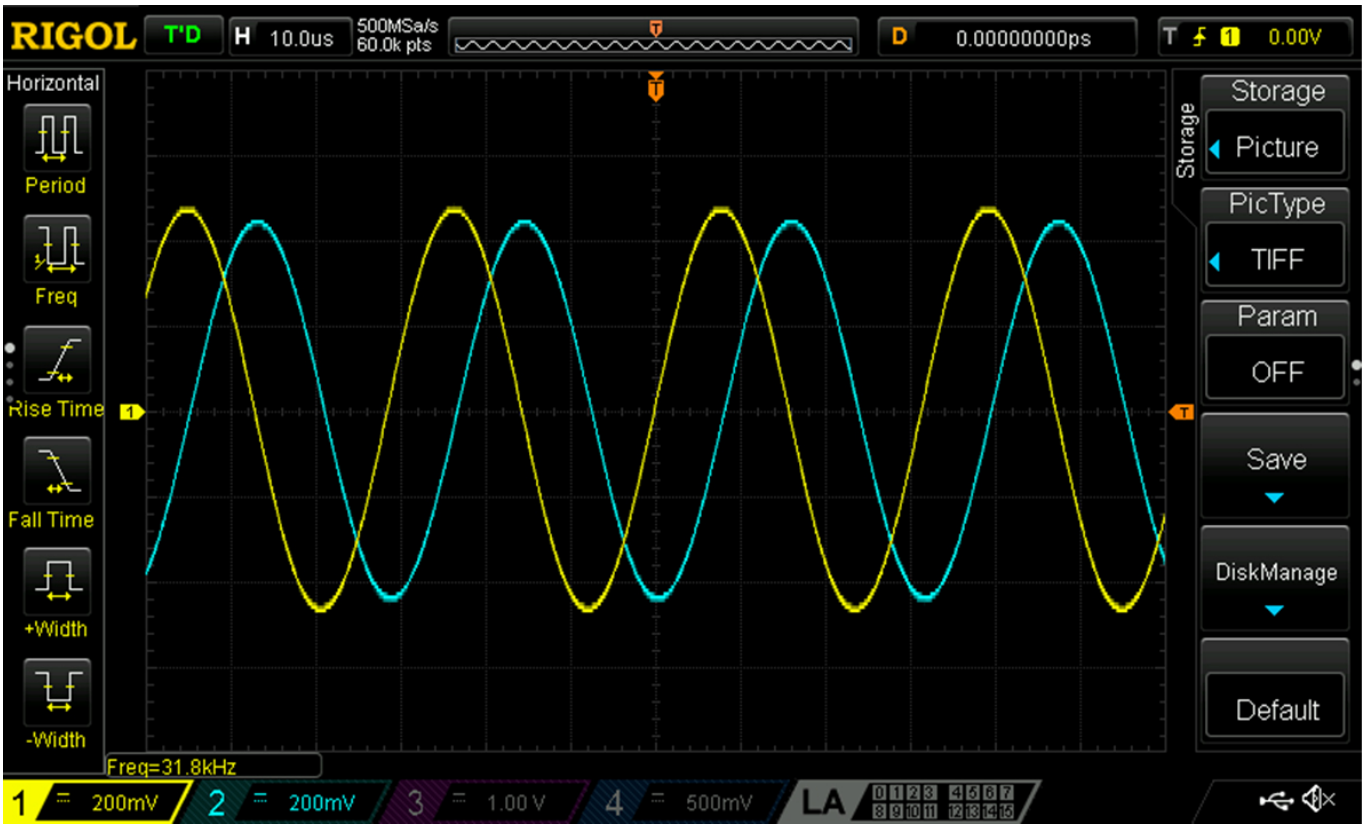

Fig. (20). Experimental transient responses of the proposed VM-FOAPF. *(A higher resolution / colour version of this figure is available in the electronic copy of the article)*.

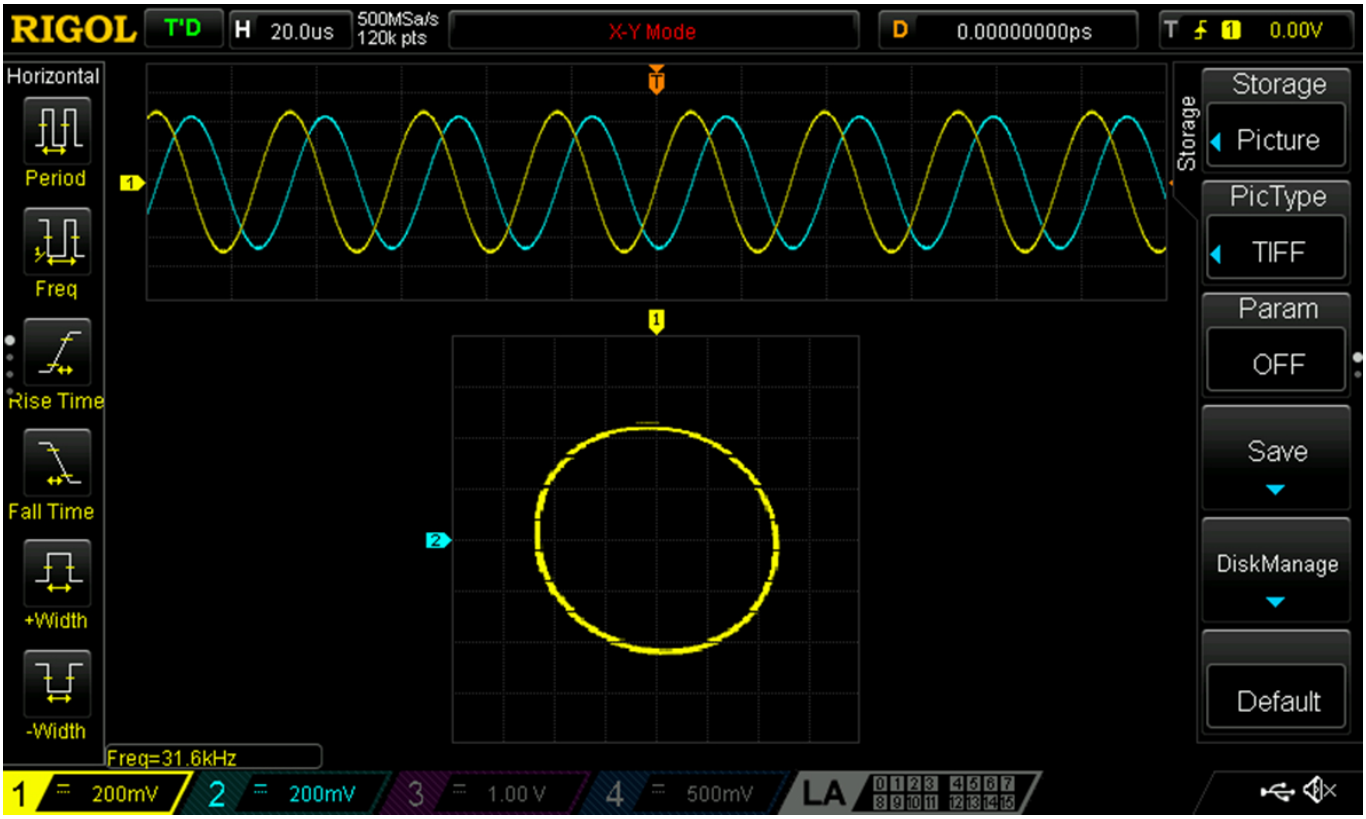

Fig. (21). Lissajous pattern of the proposed VM-FOAPF. *(A higher resolution / colour version of this figure is available in the electronic copy of the article).*

AUTHOR'S CONTRIBUTIONS

Study conception and design by Bhartendu Chaturvedi and Jitendra Mohan; Analysis and Interpretation of results by Khushbu Bansal. The first draft of the manuscript was written by Khushbu Bansal, and all authors have commented on previous versions of the manuscript. All authors reviewed the results and approved the final version of the manuscript.

LIST OF ABBREVIATIONS

ABB	=	Active Building Block
CCI	=	First Generation Current Conveyor
CCII	=	Second Generation Current Conveyor
C	=	Capacitor
ICCII	=	Inverting Second Generation Current Conveyor
CFOA	=	Current Feedback Operational Amplifier
DD-DXCCII	=	Differential Difference Dual-X Second Generation Current Conveyor
DDCC+	=	Positive Type Differential Difference Current Conveyor
DDCC	=	Differential Difference Current Conveyor
DCCII	=	Differential Second Generation Current Conveyor
DVCC	=	Differential Voltage Current Conveyor
DXCCDITA	=	Dual X Current Conveyor Differential Input Transconductance Amplifier
EXCCII	=	Extra-X Second Generation Current Conveyor
MCCII	=	Modified Second Generation Current Conveyor
OTA	=	Operational Transconductance Amplifier
R	=	Resistor
UVC	=	Universal Voltage Conveyor
VCII	=	Second Generation Voltage Conveyor
VDCC	=	Voltage Differencing Current Conveyor
VD-DIBA	=	Voltage Differencing Differential Input Buffered Amplifier

CONSENT FOR PUBLICATION

Not applicable.

CONFLICT OF INTEREST

The authors declare no conflict of interest, financial or otherwise.

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